FPGA-Based Power Quality Analyzer

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Abstract: This research focuses on the development of an FPGA-based power quality analyzer that addresses the limitations of traditional software-based systems in terms of processing speed and real-time performance. Leveraging the parallel processing capabilities of Field Programmable Gate Arrays (FPGAs), the proposed system performs real-time harmonic detection and power quality analysis. The analyzer integrates Fast Fourier Transform (FFT) IP cores, an XADC for analog-to-digital conversion, and a MicroBlaze soft-core processor to monitor voltage and current waveforms in a three-phase power system. The FFT computations enable efficient extraction of Total Harmonic Distortion (THD) and identification of power quality disturbances, such as sags, swells, and transients. By incorporating a Shunt Active Power Filter (SAPF), the system also mitigates harmonics in the power system. Experimental results demonstrate the real-time capabilities of the system, highlighting its accuracy and performance in handling power quality issues. Future work will explore improvements using a Zynq-7000 SoC for enhanced computational efficiency and reliability. *Keywords:* FFT, Harmonics, Microblaze, Vitis, Vivado, XADC, Xilinx, Zynq

Introduction

Power quality analysis plays a crucial role in ensuring the efficiency and reliability of electrical power systems. With the increasing complexity and sensitivity of modern-power systems, accurate monitoring, and analysis of power quality parameters have become essential for maintaining system stability and preventing costly disruptions.

Traditional power quality analyzers often rely on software-based solutions, which can be limited by processing speed and real-time performance. Therefore, there is an increasing need for innovative solutions that can provide fast, accurate, and real-time power quality analysis. This research aims to develop an FPGA-based power quality analyser to overcome the limitations of contemporary analyzers and improve the efficiency and effectiveness of power quality monitoring and enhance the power quality by mitigating the harmonics of a power system.

The proposed analyzer will leverage the capabilities of FPGAs to perform high-speed signal processing and analysis tasks, enabling efficient and reliable power quality monitoring. This analyser is integrated with a Shunt Active Power Filter [3][4][5] as an extension of the project on behalf of mitigating the harmonics prevailing in a 3-phase power system.

Literature Review

Power quality analyzers have become increasingly important with the proliferation of sensitive electrical devices, which are more

vulnerable to power disturbances such as harmonics, sags, swells, and transients. These disturbances can lead to energy inefficiencies, equipment damage, and system failures. The integration of FPGA technology into power quality analysis offers real-time capabilities, enhanced computational power, and greater flexibility. This section reviews previous research related to FFT implementation on FPGAs and their application to power quality analysis.

Kumar et al. [7] explored the challenges and performance metrics associated with implementing FFT algorithms on FPGAs. They detailed various algorithmic approaches, such as radix-2 and radix-4 FFTs, discussing their respective trade-offs in terms of resource utilization and processing time. The authors concluded that the inherent parallelism of FPGA architectures makes them ideal for high-speed applications like power quality monitoring. Their analysis revealed that while FPGA-based FFT implementations are more resource-efficient than their software counterparts, they are also highly dependent on the configuration of the FPGA and the optimization of the algorithm, which can significantly affect performance.Shen et al. [8] investigated the implementation of real-time power quality analyzers using FPGA technology. Their research highlighted the importance of using FFT for harmonic analysis in power systems and the benefits of FPGAs for handling large data sets in real-time. Their implementation used pipelined architecture to improve the efficiency of FFT computation, showing that FPGA-based analyzers could outperform traditional software-based systems in both speed and accuracy. They also emphasized the importance of selecting the appropriate windowing techniques to minimize spectral leakage and improve the accuracy of harmonic detection.

Further advances in power quality analysis were presented by Basu et al. [9], who implemented a power quality analyzer on FPGA with real-time harmonic detection and classification capabilities. Their study demonstrated that FPGA-based systems could effectively handle the high data throughput required for power quality monitoring by leveraging the parallel processing abilities of the hardware. Basu et al. also focused on the accuracy of harmonic detection, concluding that their FPGA-based system achieved superior performance in terms of both speed and harmonic classification when compared to software-based solutions. Additionally, Shuhui et al. [10] examined the integration of FFT in embedded systems for power quality applications. They analyzed the trade-offs between hardware resource usage and processing speed, concluding that while FPGAs can provide faster real-time analysis, optimizing the algorithm's hardware mapping is crucial for minimizing resource consumption and maximizing performance. They also highlighted the importance of using a direct memory access (DMA) interface to manage the data flow efficiently between the FFT processing unit and other system components, further enhancing the performance of the analyzer.These studies collectively indicate that FPGA-based implementations of power quality analyzers are superior to traditional software-based solutions in terms of speed, real-time performance, and accuracy. The primary

advantage of using FPGAs lies in their ability to exploit parallelism, enabling high-speed processing of FFTs for harmonic analysis and other power quality measurements. However, optimizing the FFT algorithm for hardware implementation remains a key challenge, requiring careful consideration of resource allocation, latency, and power efficiency.

Materials & Methods

This section covers the methodology followed in the research project. It encompasses all the sections of hardware and software including simulations and real-world implementation.

Developing a complete system architecture using a Microblaze Soft core processor with Xilinx Vivado

Creating a system architecture as in Figure 1 using a MicroBlazesoft-core processor within Xilinx Vivado involves integrating various components to build a functional design. The MicroBlaze processor serves as the central processing unit, orchestrating the operations of other peripheral components. In this setup, we'll be utilizing two BRAMs (Block RAMs), an XADC (Xilinx Analog-to-Digital Converter), AXI DMA (Direct Memory Access), and an FFT IP [1][2][6] (Fast Fourier Transform Intellectual Property).

The MicroBlaze processor acts as the brain of the system, executing instructions and managing the flow of data. Its flexibility and configurability make it an ideal choice for embedded systems. It communicates with the other components through a bus interface, allowing seamless data exchange and control. The BRAMs serve as on-chip memory units, providing fast access to data for the processor. They store both program instructions for the MicroBlaze and temporary data during processing. The XADC module enables the system to interface with analog signals, converting analog inputs into digital data that can be processed by the MicroBlaze or stored in memory. The AXI DMA controller facilitates efficient data transfer between different peripherals and memory. It allows for high-speed data movement without involving the processor directly, which enhances system performance. The FFT IP core [2] is a specialized module designed to perform fast Fourier transforms [4][6], a crucial operation in signal processing, data analysis, and various other applications. This IP core can execute FFT algorithms efficiently, processing incoming data and providing frequency domain information. Integrating these components within Vivado involves designing and configuring the system architecture using block diagrams, IP integrations, and interconnections between the modules. Each component's interface, data flow, and control signals need to be appropriately managed and connected to ensure proper functionality. First data from the current sensor ACS712 connected to FPGA PMOD pin 1 of the JXADC section of pins is taken into the processing by the JXADC of Basys3 FPGA board. This data is taken in by the channel 6 of the XADC which is operating in the channel sequencer mode with a sampling rate of 50KSPS (kilo samples per second). This configuration is for one phase and for three-phase operation, two other channels and two other PMOD pins associated with

those channels should be selected.

Rest of the architecture explained below stays the same with no difference.

Then this sampled data which is now in the digital domain is then directed to the storage in first block RAM temporarily. This data is in 16 bits and is then directed to the FFT IP for calculating the Fourier values for the samples. The FFT has a transform length of 1024 and a clocking frequency of 100MHz. These values are moved to FFT thorugh AXIDMA IP. It is necessary to use this block because the data coming from the blockram is in AXI Memory Map and the FFT only accepts Stream data. So, there should be conversion between these data protocols. AXIDMA IP is capable of doing this.

AXI Memory Map and AXIS Stream

The AXI Memory Map protocol is typically used for standard data transfers between memory and peripherals, where the memory addresses are specified for read/write operations. In contrast, the AXIS Stream protocol is used when continuous data streaming is required, such as in the case of real-time data processing.

The FFT IP block accepts data only in AXIS Stream format, while data in the Block RAM (BRAM) is stored in AXI Memory Map format. Therefore, to transfer the data from the BRAM to the FFT IP, a protocol conversion is necessary.

This is accomplished through the AXI DMA IP core, which converts the AXI Memory Map data from BRAM into AXIS Stream data for the FFT IP. Similarly, after the FFT processing, the AXIS Stream data is converted back into AXI Memory Map format before being written into another BRAM. This conversion is handled by the AXI DMA IP block, ensuring smooth transitions between the two protocols without processor involvement.

After this is done, the calculated Fourier values from FFT IP which are in AXIS Stream protocol are transferred to the other blockram via AXIDMA. Here the protocol change happens from AXIS Stream to AXI Memory Map. These calculated values are displayed through Xilinx Vitis terminal. In the hardware architecture AXI UARTLITE block has a baudrate of 115200.

Coding the processor using Xilinx Vitis in C for Harmonic extraction

Once the architecture is established, the next step involves writing code for the MicroBlaze processor, configuring the peripherals, and establishing communication protocols between the components and doing necessary calculations for THD. Additionally, the system requires verification, simulation, and debugging to ensure proper operation. Here the coding needs the libraries for XADC, AXIDMA, Complex etc. The coding is done in C. This code is stored in the processor memory for conducting systemâĂŹs operations.

Coding the processor with Xilinx Vitis in C for SAPF operation

Rest of the algorithms required like Current control algorithm, synchronizing algorithm and DC-Link capacitor voltage regulation algorithm are implemented in C in Vitis. The procedures implemented are Simulating the proposed

circuitry for SAPF with Matlab and Proteus for proper values of the components, the SAPF, Testing SAPF, and Measuring the Current.

An analog current sensor ACS712 is used and connected with PMOD pin 1 of the JXADC section of pins for JXADC of Basys3 FPGA board. This reading is then calibrated in the coding for Microblaze processor in Xilinx Vitis. In this way analog sensor value for the current is converted to digital domain.

Results & Discussions

This methodology used in cooperating a Microblaze soft core processor is far advanced in comparison to merely coding with Verilog. Though we were able to implement the complete architecture and coding, and we could direct the signal into the FPGA and do ADC conversion and store in Block RAM memory, we became unable to direct these stored values through AXIDMA. The system architecture design validates with no errors and Synthesis, Implementation and Bit stream generation happen with no issue.

The integration of AXI DMA and FFT IP posed significant challenges during the design phase of the FPGA-based Power Quality Analyzer. The AXI DMA IP core, which facilitates the transfer of data between the AXI Memory Mapped (BRAM) and AXIS Stream (FFT IP) formats, requires proper synchronization and configuration for efficient data handling. While AXI DMA offers high-speed data transfers, achieving the required real-time performance was difficult due to the inherent latency in the data stream. Configuring the AXI DMA to precisely align the data packets for the FFT IP block often resulted in timing violations, which degraded the overall system performance. Managing data buffers between AXI DMA and the FFT IP core proved complex. The FFT IP requires continuous data streaming, which was not always possible to guarantee with AXI DMA due to buffering delays and mismatches in data size expectations between the blocks. The FFT IP block requires input in a specific data format (complex numbers in fixed-point representation). Ensuring that the data sent from the AXI DMA is in the correct format often led to issues with data precision and accuracy, complicating the integration further.

So, to mitigate this issue, different approach was tried.

Coding FFT IP in Processor memory

The solution was to code the FFT in processor memory from scratch. But this discarded the efficiency which can be achieved by the FFT IP which is solely dedicated for FFT calculation.

By coding the FFT in processor memory, we gained full control over data handling, formatting, and processing. The processorâĂŹs ability to manage data transfers directly allowed us to bypass the complexity of AXI DMA and avoid synchronization issues. In processor memory, data could be stored and processed sequentially without the need for real-time streaming. This eliminated the need for continuous data handling and minimized the risk of data packet loss or format mismatch.

Implementing the FFT in software made debugging simpler because traditional software debugging tools could be used to analyze the data flow, identify issues, and verify the accuracy of the FFT computations.

While this solution resulted in slightly lower performance compared to a fully hardware-based approach, the reliability and ease of

implementation made it a viable alternative, especially for prototyping. The flexibility offered by the processor memory outweighed the potential performance gains of using the FFT IP under the AXI Stream protocol.
The following values were calculated as the result for a given wave form.

```
What would you like to do?
0: Print current FFT parameters
1: Change FFT parameters
2: Perform FFT using current parameters
3: Print current stimulus to be used for the FFT operation
4: Print results of previous FFT operation
5: Quit
xn(0) = 6041 + j*0
xn(1) = 6039 + j*0
xn(2) = 6037 + j*0
xn(3) = 6067 + j*0
xn(4) = 6156 + j*0
xn(5) = 6196 + j*0
xn(6) = 6233 + j*0
xn(7) = 6277 + j*0
xn(8) = 6352 + j*0
xn(9) = 6342 + j*0
xn(10) = 6403 + j*0
xn(11) = 6501 + j*0
xn(12) = 6477 + j*0
xn(13) = 6469 + j*0
xn(14) = 6535 + j*0
xn(15) = 6534 + j*0
xn(16) = 6476 + j*0
xn(17) = 6413 + j*0
xn(18) = 6334 + j*0
xn(19) = 6319 + j*0
xn(20) = 6280 + j*0
xn(21) = 6329 + j*0
xn(22) = 6272 + j*0
xn(23) = 6243 + j*0
xn(24) = 6196 + j*0
```

Figure 8: Calculated Fourier Values

The performance comparison between the FPGA-based and software-based analyzers is a critical aspect of this study, and this analysis is still ongoing. The primary focus is to evaluate the real-time processing capabilities and latency between the two approaches. The FPGA-based analyzer leverages custom hardware acceleration to perform high-speed real-time signal processing. Profiling will be conducted using Vitis, where the system's performance will be analyzed in terms of latency, throughput, and resource utilization. By monitoring key performance metrics in Vitis, we can evaluate the efficiency of the hardware implementation and identify any potential bottlenecks. The profiling process in Vitis will focus on;

Latency measurements - The time taken for the entire FFT computation and data transfer from input to output, including the effects of AXI DMA and AXIS Stream.

Throughput - The rate at which data is processed through the FPGA system, particularly in handling real-time power signals.

Resource utilization - Analysis of LUTs, DSP slices, and BRAM usage to determine the hardware efficiency.

For the software-based analyzer, performance will be assessed by running the same FFT and signal processing algorithms on a CPU, likely using a standard real-time operating system or a bare-metal implementation. The performance will be evaluated based on the processing time per signal frame and the system's ability to handle continuous real-time data without dropping packets or exceeding acceptable latency thresholds.

The ongoing comparison will involve running real-time benchmarks on both platforms, capturing performance data using the aforementioned metrics. Detailed results will be presented in future work, with a focus on illustrating the advantages and trade-offs between the FPGA-based and software-based analyzers for real-time power quality monitoring.

Using Zynq 7000 SoC with Zybo Master FPGA

This will solve the persisting issues with Microblaze processors.

Power Quality Analysis and FFT

Power quality refers to maintaining a stable and pure sinusoidal waveform of voltage and current within an electrical system. Any deviation from the ideal sinusoidal waveform, including the presence of harmonics, transients, sags, and swells, can indicate power quality issues that may cause malfunctioning of electrical equipment or inefficiencies in energy usage.

For a periodic signal, the Fourier series represents the signal as a sum of sinusoidal components with different frequencies. The FFT is a computationally efficient algorithm to compute the Discrete Fourier Transform (DFT) of a signal, which breaks the signal into its frequency components.

Given a discrete time-domain signal $x[n]$ of length N, the DFT is defined as:

$$X[k] = \sum_{n=0}^{N-1} x[n] \cdot e^{-j\frac{2\pi}{N}kn}$$

Where:

- $X[k]$ represents the magnitude of the k-th frequency component.
- n is the time-domain index.
- k is the frequency index (from 0 to $N-1$).
- j is the imaginary unit.

In power quality analysis, these frequency components are critical because they help detect harmonics. Harmonics are multiples of the fundamental frequency (50 Hz) that appear in the signal due to distortions from non-linear loads.

Using FFT, we can calculate the Total Harmonic Distortion (THD), which is a key indicator of power quality. THD quantifies the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency;

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + \cdots + V_n^2}}{V_1}$$

Where:

- V_1 is the RMS voltage of the fundamental frequency.
- $V_2, V_3, \ldots, V_n$ are the RMS voltages of the harmonic components.

The lower the THD, the better the power quality of the system. A higher THD indicates significant waveform distortion and potential issues with power quality.

In the FPGA-based Power Quality Analyzer, the FFT is applied to the voltage and current signals sampled by the XADC. By performing FFT on these signals, the system identifies the magnitude of the fundamental frequency and the harmonics. This enables the real-time detection of power quality issues such as:

Harmonics - Distortions that result in inefficient energy consumption and possible equipment damage.

Voltage Sags and Swell - Deviations from nominal voltage levels, which can be identified by sudden changes in the fundamental frequency magnitude.

Transients - Short-duration disturbances that occur when there are abrupt changes in the load or during switching events.

With the FFT's frequency-domain representation, the analyzer can detect deviations from ideal conditions and provide

insights into the underlying causes of power quality issues.

Conclusions & Recommendations

It was concluded that by using Basys 3 FPGA the detection of harmonics of the power system can be detected. Furthermore, it was concluded the delay in detection of the harmonic is negligible due to the 100MHz clock speed of the board.

Future Work

The inability to use the FFT IP core using the design associated with Microblaze is a drawback with Basys 3. To mitigate this issue an FPGA with a Zynq 7000 SoC can be used. Therefore, the design has to be changed and can be implemented in a Zybo Z7 FPGA.

Rest of the algorithms to operate Shunt Active Power Filter [3] [4] [5] should be developed with Verilog HDL and should be interfaced with this architecture. Shunt Active Power Filter [4] hardware should be developed for future work.

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